Day 1 | 19 Nov 2023 | Sunday				
Start	**End**	**Duration**	**Session 1 (5th Floor) [PRIME Asia]**	**Session 2 (5th Floor) [PRIME Asia]**
8:30	9:00	0:30	**Welcome/Registration (Ground Floor)**	
9:00	9:30	0:30	**Opening Session**	
9:30	11:00	1:30	**T1: Why Standards Matter: Impact and Importance of IEEE Standards** Srikanth Chandrasekaran, Sr. Director, IEEE	**T2: Machine Learning in EDA Tool Development: An FPGA Based Study** Dinesh Bhatia, University of Texas at Dallas, USA
11:00	11:30	0:30	**Tea / Coffee Break**	
11:30	13:00	1:30	**T3: Design-For-Manufacturability for Nano-Scale CMOS Technology** Yongfu Li, Shanghai Jiao Tong University	**T4: Selecting the Right Topology of Voltage Regulators for Your System** Qadeer Khan, IIT Madras
13:00	14:00	1:00	**Lunch Break**	
14:00	15:30	1:30	**T5: Multi-channel Delta-Sigma Analog-to-Digital Converters Without Reset** AshwinKumar Ramakrishnan Sivakumar, IIT Kanpur and Nagendra Krishnapura, IIT Madras	**T6: A Reliable and Robust Framework for Accurate Timing Sign-Off with Reduced Design Margin of Digital Integrated Circuits** Anand Bulusu, IIT Roorkee
15:30	16:00	0:30	**Tea / Coffee Break**	
16:00	17:30	1:30	**Industry Tutorial 1: Building Energy Efficient Wireless Semiconductors and Systems** Joseph Kolapudi, Silicon Labs	**Industry Tutorial 2: Design, Test and Calibration of High-accuracy CMOS Temperature Sensors** Sudhakar Singamala and Rajashekar Benjaram, ams OSRAM
17:30	18:00	0:30	**Tutorials Closing Ceremony**	

Start	End	Duration	Session 1 (5th Floor)	Session 2 (5th Floor)	Session 3 (6th Floor)	Location
Day 2 | 20 Nov 2023 | Monday						
8:30	9:00	0:30	**Welcome/Registration**			**Ground Floor**
9:00	10:00	1:00	**Inauguration Ceremony** **Shri. Ajay Kumar |Distinguished Professor, IIT Kanpur (Former Defence Secretary, Govt. of India)** **Dr. Reiner Jumpertz | Senior Vice-President and General Manager, ams OSRAM**			**5th Floor**
10:00	10:30	0:30	**Keynote Talk: Five Cyber Security Woes That Threaten Digital India and Proposed Action Plan to Deal with Them** **Shri. Ajay Kumar | Distinguished Professor, IIT Kanpur (Former Defence Secretary, Govt. of India)**			
10:30	11:00	0:30	**Keynote Talk: Optical Sensors Seeing the Unseen and Beyond** **Dr. Reiner Jumpertz | Senior Vice-President and General Manager, ams OSRAM**			
11:00	11:30	0:30	**Inauguration of Exhibition, Tea / Coffee Break**			**Ground Floor**
11:30	12:30	1:00	**Panel Discussion: Accelerating Innovation in Indian Semiconductor Eco-system** **Rajesh Gupta | Country Head, Sr. Director, ams OSRAM** **Sarat Vetcha | Director EP SW R&D, NXP** **Manish Hooda | Head Technology Development Division, SCL Mohali** **Jatinder Singh | Senior Business Development Manager, IMEC** **Alex James | Professor, Digital University Kerala (Moderator)**			**5th Floor**
12:30	13:00	0:30	**Celebration: 75 Years of CASS** **Amara Amara | CASS Past President** **Yoshifumi Nishio | Tokushima University, Japan** **Fakhrul Zaman Rokhani | Education Committee Chair, IEEE** **PA Govindcharulu | Director, Manjeera Digital Systems** **Preet Yadav | R & D SoC Technical Program Manager, NXP**			
13:00	13:50	0:50	**Lunch Break**			**Ground Floor**
			Technical Papers Session: 1A **Analog and Mixed Signal Design** **Session Chair: Anand Bulusu | IIT Roorkee** **Invited Talk: Performance and Reliability Analysis of a Stacked Nanosheet/Forksheet for Device Circuit Co-design** **Sudeb Dasgupta | Professor, IIT Roorkee**	**Technical Papers Session: 1B** **Neuromorphic Circuits** **Session Chair: Dinesh Bhatia | UT Dallas** **62**: Energy Efficient DSHE based Analogue Multiply Accumulate Computing Crossbar Architecture [Sandeep Soni (Indian Institute of Technology Roorkee); Gaurav Verma (Indian Institute of Technology Roorkee); Alok Kumar Shukla (Indian Institute of Technology Roorkee); Brajesh Kumar Kaushik (Indian Institute of Technology Roorkee)]	**Technical Papers Session: 1C** **Digital Circuit Design & System Architecture** **Session Chair: Rajesh Zele | IIT Bombay** **58:** FPGA Implementation of Inversion in Galois Field Over GF(2^m) with FLT and ITA using Quad Blocks [Vemanaboina Vamsi (IIT-BHU); Kishor Prabhakar Sarawadekar (IIT-BHU)]	
			95: A Double Cross-Coupled Delay Cell for High-Frequency Differential Ring VCOs [Mayank Kumar Singh (Indian Institute Of Technology Ropar); Manish Kumar Gautam (Indian Institute of Technology Ropar); Puneet Singh (Indian Institute of Technology Ropar); Raja Sekhar Nagulapalli (Oxford Brookes University Wheatley Campus Oxford, United Kingdom); Devarshi Mrinal Das (Indian Institute of Technology Ropar); Mahendra Sakare (Indian Institute of Technology Ropar)]	**90:** Energy Efficient Memristor-based Subtractors and Comparator for In-Memory Computing in MAGIC [Nandit Kaushik (Indian Institute of Technology, Mandi); Srinivasu Bodapati]	**71:** An FPGA based Accelerator of the Bi-directional Wavefront Algorithm for Pairwise Sequence Alignment [Ajay S (Indian Institute of Science); Praveen V S (Indian Institute of Science); Kuruvilla Varghese (Indian Institute of Science)]	

13:50	15:30	1:40	**130:** A 17 GHz Output PLL-Based Frequency Doubler with -60dBc Fundamental Spur Soumith Kusumanchi (IIT Madras, Texas Instruments India); Srinivas Theertham (Texas Instruments India); Arpan Thakkar (Texas Instruments India); Nagendra Krishnapura (IIT Madras)	**195:** 3.6- pJ /spike, 30-Hz Silicon Neuron Circuit in 0.5-V, 65 nm CMOS for Spiking Neural Networks [Srikanth Vuppunuthala (Indian Institute of Technology Bhubaneswar); Vijay Shankar Pasupureddi (Indian Institute of Technology Bhubaneswar)]	**88:** Ternary Systolic Array Architecture for Matrix Multiplication in CNFET-Memristor Technology [Srinivasu bodapati; Shivani Thakur (IIT Mandi)]	**Session 1 & 2: 5th Floor** **Session 3: 6th Floor**
			179: Settling Time Reduction in a Phase-Locked Loop using Pre-emphasis Sumit Kumar (IIT Madras); Nagendra Krishnapura (IIT Madras)	**258:** A Bio-Inspired CMOS Circuit for the Excitation and Inhibition of Neuronal Oscillators [BharathKumarSingh Muralidhar (Christian-Albrechts-UniversitätzuKiel); Bakr Al Beattie (Ruhr-University Bochum); Max Uhlmann (IHP - Leibniz-Institut fur innovative Mikroelektronik); Karlheinz Ochs (Ruhr-University Bochum); Gerhard Kahmen (IHP - Leibniz-Institut fur innovative Mikroelektronik); Robert Rieger (University of Kiel)]	**120:** A 1-kb Sub-1 fJ/b per Access CAM Design Using 40-nm CMOS Process [Ralph Gerard B. Sangalang (National Sun Yat-Sen University); Wei-Zhen Chen (National Sun Yat-Sen University); Chua-Chin Wang (National Sun Yat-Sen University)]	
			194: A 1-6 GHz, Sub-mW Self-Aligned Quadrature Phase Clock Generator in 1.2 V, 65 nm CMOS Raviteja Kammari (Indian Institute of Technology Bhubaneswar); Sarvesh Rajesh Tuckely (Indian Institute of Technology Bhubaneswar); Vijay Shankar Pasupureddi (Indian Institute of Technology Bhubaneswar)	**64:** Investigation of Voltage Fault Injection Attacks on NN Inference Utilizing NVM based Weight Storage [Supriya Chakraborty (Indian Institute of Technology Delhi); Tamoghno Das (Indian Institute of Technology Delhi); Manan Suri (IIT-Delhi)]	**159:** True Random Number Generator implemented in ReRAM Crossbar based on static stochasticity of ReRAMs. [Tanay Patni (Department of Electrical and Electronics Engineering BITS Pilani K. K. Birla Goa Campus); Abhijit Pethe (BITS Pilani)]	
15:30	16:00	0:30	**Tea / Coffee Break**			**Ground Floor**
16:00	16:30	0:30	**Keynote Talk: A Stochastic Computing Approach to Low Latency, High Efficiency Accelerators for Edge ML Applications** **Sudhakar Pamarti | Professor, University of California, Los Angeles**			**5th Floor**
16:30	17:00	0:30	**Keynote Talk: On-chip Spectral Imaging: Enabling Novel Applications for a Brighter Future** **Wouter Charle | Program Manager, IMEC**			

Start	End	Duration	Session 1	Session 2	Session 3	
Day 3 | 21 Nov 2023 | Tuesday						
8:30	9:00	0:30	**Welcome/Registration**			**Ground Floor**
9:00	9:30	0:30	**Keynote Talk: Continuous-Time Pipelined Converters- Where Filtering Meets Anlog-to-Digital Conversion** **Shanthi Pavan | NT Alexander Institute Chair Professor, IIT Madras**			**5th Floor**
9:30	10:00	0:30	**Keynote Talk: Circuits and Systems: How Smart is Smart and How Safe is Safe?** **Girishankar Gurumurthy | Deputy Directory, Technology - Compute and Artificial Intelligence Group, MediaTek**			
10:00	10:30	0:30	**Tea / Coffee Break and Poster Session 1***			**Ground Floor**
10:30	11:30	1:00	**Industry Forum (PRIME Asia)** **Session Chair: Preet Yadav | NXP** **Research Driven Cybersecurity: DSCI's Perspective** **Teja Chintalapati | Senior Program Manager, DSCI**	**Technical Papers Session: 2B (PRIME Asia)** **Late Breaking Category** **Session Chair: Kala S | IIT Kottayam** **5:** An Innovative Write Circuitry for Enhancing a 3nm L1 Cache Performance Across Wide DVFS Range [Sandipan Sinha (Mediatek Bangalore Pvt. Ltd.); Manish Trivedi (Mediatek Bangalore Pvt. Ltd.); Jaswinder Singh Sidhu (Mediatek Bangalore Pvt. Ltd.); Sriharsha Enjapuri (Mediatek Bangalore Pvt. Ltd.); Deepesh Gujjar (Mediatek Bangalore Pvt. Ltd.); Ramesh Halli (Mediatek Bangalore Pvt. Ltd.); Girishankar Gurumurthy (Mediatek Bangalore Pvt. Ltd.)] **16:** A correlation based adaptation (CBA) for Efficient Implementation of Golomb-Rice Encoding [Vijay Joshi (Indian Institute of Space Science and Technology); Soham Maiti (Indian Institute of Space Science and Technology); Savio Sebastian (Indian Institute of Space Science and Technology); Dr. J Sheeba Rani (Indian Institute of Space Science and Technology); Dipika Simeria (Indian Institute of Space Science and Technology)]	**Technical Papers Session: 2C (PRIME Asia)** **Special Session** **Session Chair: Sim Narasimha | Stanford University** **30:** FPGA-targeted optimization approaches for SVM and CNN human activity recognition models using the HARTH and HAR70+ datasets [Ramona Rajagopalan (University of the Philippines Diliman); Ian Palabasan (University of the Philippines Diliman); Maria Theresa De Leon (University of the Philippines Diliman); John Richard Hizon (University of the Philippines Diliman); Marc Rosales (University of the Philippines Diliman); Jean Marriz Manzano (University of the Philippines Diliman)] **33:** A 4-kHz per °C High Linearity On-chip Temperature Sensor Implemented Using 40-nm CMOS Process [Ralph Gerard Bolina Sangalang (Batangas State University and National Sun Yat-Sen University); Chi-Lin Lee (National Sun Yat-Sen University); You-Wei Shen (National Sun Yat-Sen University); Celso Bastion Co (Batangas State University); Chua-Chin Wang (National Sun Yat-Sen University)]	**Session 1 & 2: 5th Floor** **Session 3: 6th Floor**

			Wireless Technologies and the Growth of Digitalization **Venkatesh Narasimhan | Silicon Labs**	20: A 35 pW, 19.23 ppm/◦C Dual Self-Regulated CMOS Voltage Reference for Energy Autonomous IoT Devices [Raghav Bansal (Indian Institute of Technology Delhi); Sweta Tripathi (Indian Institute of Technology Delhi); Shouri Chatterjee (Indian Institute of Technology Delhi)]	**34:** A 9-bit 2MS/s Set-and-Down Monotonic SAR ADC in 22nm-FDSOI for MEMS-based Thermoelectric Sensor Readout Circuit [Maria Sophia C. Ralota (University of the Philippines Diliman); Arcel Leynes (University of the Philippines Diliman); Maria Theresa G. de Leon (University of the Philippines Diliman)]	
				26: Digital Background Calibration Technique to Mitigate Vertical FPN in CMOS Image Sensors [Bibhudutta Satapathy (Indian institute of technology, jodhpur); Pratham chaurasia (Indian institute of technology , jodhpur); Amandeep Kaur (Indian Institute of Technology Jodhpur)]		
				40: Enhancing Linearity and Efficiency in Multi-Bit MAC Computation for Convolution in DNNs Using SRAM Array [VINOD PATHLOTH (Deputy Manager, Tube Investments of India); Kavitha Soundra pandiyan (Research scholar); Bhupendra Singh Reniwal (Indian Institute of Technology Jodhpur)]		
11:30	**13:10**	**1:40**	**Industry Forum (PRIME Asia)** **Session Chair: A G. Krishna Kanth | amsOSRAM** **CXL Memory Use Case for Data Center SSD Application** **Rajesh Maruti Bhagwat | Sr. Technical Manager, Micron** **ASIC Advanced Packaging and Test** **Peter Dirks | Asic Project Manager, IMEC** **Differentiation with RISC-V processors in Edge-Computing** **Sourav Roy, Fellow, NXP**	**Technical Papers Session: 4B** **IoT, Intelligent Circuits and Systems** **Session Chair: Harini Kandadai | ams OSRAM** **175:** TinyRadar for Gesture Recognition: A Low-power System for Edge Computing [Dileep Kankipati (IISc, Bangalore); Madhu Munasala (IISc, Bangalore); Nikitha Sai Dasari (IISc, Bangalore); Satyapreet Yadav (Indian Institute of Science); Sandeep Rao (Texas Instruments, Bangalore); Chetan Singh Thakur (IISc, Bangalore)]	**Technical Papers Session: 4C** **Digital Circuit Design & System Architecture** **Session Chair: Qadeer Khan | IIT Madras** **Invited Talk: Towards AGI Chips - Why, What and How** **Alex James | Professor, Digital University Kerala**	**Session 1 & 2: 5th Floor** **Session 3: 6th Floor**
				219: Novel Label Flipping Dataset Poisoning Attack Against ML-based HT Detection Systems [Richa Sharma (Ph.D scholar, ABV-IIITM, Gwalior); G.K. Sharma (ABV-IIITM, Gwalior, India); Manisha Pattanaik (ABV-IIITM, Gwalior, India)]	**246:** Power-Efficient Approximate Multipliers Leveraging Hybrid CMOS-Memristor Paradigm [Monika Pokharia (Indian Institute of Technology, Gandhinagar); Ravi Sadanand Hegde (Indian Institute of Technology, Gandhinagar); Joycee M. Mekie (Indian Institute of Technology Gandhinagar)]	
				227: LOKI: A Secure FPGA Prototyping of IoT IP with Lightweight Logic Locking [Jugal Gandhi (AcSIR at CSIR-CEERI); Diksha Shekhawat (AcSIR at CSIR-CEERI); M. Santosh (CSIR-CEERI); Jai Gopal Pandey (CSIR-CEERI)]	**255:** ABB Assisted Area Efficient Vernier Delay Line Time-to-Digital Converter for Low voltage Application [Ravi Singh (IIT Roorkee); Lomash Chandra Acharya (IIT Roorkee); Mahipal Dargupally (IIT Roorkee); Neha Gupta (IIT Roorkee); Neeraj Mishra (IIT ROORKEE); Lalit Dani (GlobalFoundries); Nilotpal Sarma (IIT Roorkee); Devesh Dwivedi (GlobalFoundries); Sudeb Dasgupta (Professor, IIT Roorkee); Anand Bulusu (Indian Institute of Technology Roorkee)]	
				231: Power Efficient Hardware Fingerprint: Exploiting Process-Variations in A Quasi-Planar 14nm FinFET [Jyoti Patel (Indian Institute of Technology Roorkee); Govind Sharma (NIT, Uttarakhand); Chitraja Rajan (Shree Ramdeobaba College of Engineering and Management, Nagpur, Maharashtra); Vivek Kumar (NIT Uttarakhand & IIT Roorkee); Sudeb Dasgupta (Professor, IIT Roorkee)]	**262:** An Efficient Standard Cell Design Methodology by Exploiting Body Biasing and Poly Biasing in FDSOI for NTV Regime [Mahipal Dargupally (IIT Roorkee); Lomash Chandra Acharya (Indian Institute of technology,roorkee); Khoirom Johnson Singh (Indian Institute of Technology Roorkee); Neha Gupta (Indian Institute of Technology Roorkee); Arvind Sharma (IMEC); Sudeb Dasgupta (Professor, IIT Roorkee); Anand Bulusu (Indian Institute of Technology Roorkee)]	

				93: Passive RF Resonant Receiver with Voltage Gain for Wireless Power Transfer System [Vikas Kumar (IIT Delhi); Santosh Parajuli (CARE, IIT Delhi); Shivansh Awasthi (CARE, Indian Institute of Technology Delhi); Gayatri Ranade (Department of Biological and Chemical Engineering, University at Buffalo NewYork, USA); Kartik Tyagi (Centre for Applied Research in Electronics (CARE, IIT Delhi); Saheli Roy Chowdhury (CARE, IIT Delhi); Rahul Jaiswal (CARE, IIT Delhi); Thomas George Thundat (Department of Biological and Chemical Engineering, University at Buffalo NewYork, USA); Ankur Gupta (Centre for Applied Research in Electronics (CARE), IIT Delhi)]	**274:** Reinforcement learning based Prefetch-Control Mechanism [Soma Ghosh (Malaviya National Institute of Technology)]	
13:10	**14:00**	**0:50**	**WiCAS : Networking, Design Contest Demonstration (Ground Floor) & Lunch Break (5th Floor)**			**5th Floor**
14:00	**15:40**	**1:40**	**Women in Circuits and Systems (WiCAS) Forum** **Session Chair: Harini Kandadai | ams OSRAM** **Sumedha Limaye | Vice President of Engineering, Intel** **Usha Gogineni | Director, ams OSRAM** **Vijayalatha | IEEE** **Yarlagadda Padma Sai | IEEE**	**Technical Papers Session: 3B** **Circuits & Systems for DSP, AI & Deep Learning** **Session Chair: Nagendra Krishnapura | IIT Madras** **42:** Digital to Pulse Converter for Analog in Memory Compute Applications [Sanmitra Naik (Globalfoundries Engineering Pvt. Ltd.); Asif Iqbal (GlobalFoundries Engineering Private Limited)]	**Technical Papers Session: 3C** **Digital Circuit Design & System Architecture** **Session Chair: Santhosh Sivasubramani | IEEE** **178:** CAWPR: Contention Aware Write Preemptive Management Policy for Hybrid Last Level Caches [Swatilekha Majumdar (Indian Institute of Technology Delhi)]	**Session 1 & 2: 5th Floor** **Session 3: 6th Floor**
				73: SPARCI: Sparse Acceleration of RISC-V-based Convolutional Neural Networks for Inference using Winograd Transformation [Shabirahmed Jigalur (NATIONAL YANG MING CHIAO TUNG UNIVERSITY); Chang-Ling Tsai (NATIONAL YANG MING CHIAO TUNG UNIVERSITY); Yu-Chi Shih (NATIONAL YANG MING CHIAO TUNG UNIVERSITY); Yen-Cheng Kuan (NATIONAL YANG MING CHIAO TUNG UNIVERSITY)]	**180:** Harnessing Hybrid Clock Tree Topology to Boost PPA in Highly Utilized Designs [Pallapu Lakshmi Sarvaani (IIT Tirupati); A Subba Ramkumar reddy (Intel India Pvt Ltd); Vikram Kumar Pudi (IIT Tirupati)]	
				76: Bit-Flip Attack Detection for Secure Sparse Matrix Computations on FPGA [Noble G (Indian Institute of Information Technology Kottayam, Kerala, India); Nalesh S (Cochin University of Science and Technology, Kochi, India); Kala S (Indian Institute of Information Technology Kottayam)]	**209:** All Digital Minimum Energy Point Detection for Ultra Low Power CMOS Circuits [Purvi Patel (DAIICT); Biswajit Mishra (DAIICT Gandhinagar)]	
				101: Multi Bit Compute in memory architecture using a C-2C ladder network [Jaya Kumar Abotula (Indian Institute of Technology Roorkee); Dinesh Kushwaha (Indian Institute of Technology Roorkee); Rajat Kohli (NXP Semiconductors); Jwalant Mishra (NXP Semiconductors); Sudeb Dasgupta (Indian Institute of Technology Roorkee); Anand Bulusu (Indian Institute of Technology Roorkee)]	**215:** Efficient Hardware Design of Parameterized Posit Multiplier and Posit Adder [Sadhu Sai Ram (Indian Institute of Science); Kuruvilla Varghese (Indian Institute of Science)]	
				157: A Low-Power Charge-Domain Bit-Scalable Readout System for Fully-Parallel Computing-in-Memory Accelerators [Jun Liu (Xidian University); Fuyi Li (Xidian University); Rui Xiao (Zhejiang University); Kejie Huang (Zhejiang University); Yongfu Li (Shanghai Jiao Tong University); Hao Yu (Southern University of Science and Technology); Wei Mao (Xidian University)]	**225:** Design and Characterization of Quantum Cellular Automata (QCA) based Optimized Circuits for Emerging Technologies [Sourav Karmakar (IIIT Hyderabad); Anshu Sarje (IIIT Hyderabad); Aftab Hussain (IIIT Hyderabad)]	
15:40	**16:10**	**0:30**	**WiCAS : Networking & Tea / Coffee Break and Poster Session 2***			**Ground Floor**
16:10	**17:10**	**1:00**	**WiCAS Panel Discussion: Diversity and Inclusion in Circuits & Systems for Emerging Technologies** **Usha Gogineni | Director, ams OSRAM** **Sumedha Limaye | Vice President of Engineering, Intel** **Y. Vijayalatha | IEEE** **Yarlagadda Padma Sai | IEEE** **Preet Yadav | R & D SoC Technical Program Manager, NXP (Moderator)**			**5th Floor**
17:10	**17:30**	**0:20**	**Networking Break**			**Ground Floor**
17:30	**19:30**	**2:00**	**Awards Ceremony & Cultural Evening** **Chief Guest: Hitesh Garg | Vice President & India Country Manager, NXP Semiconductor**			**7th Floor**
19:30	**21:00**	**1:30**	**Gala Dinner**			**5th Floor**

Start	End	Duration	Session 1	Session 2	Session 3	
Day 4 | 22 Nov 2023 | Wednesday						
9:00	9:30	0:30	**Welcome/Registration**			
9:30	10:00	0:30	**Keynote Talk** **Dr.Venu Kandadai | Founder and CEO, Manjeera Digital Systems**			
10:00	11:00	1:00	**Panel Discussion: Industry-Academia Collaboration for the Future Semiconductor Challenges** **Sanjay Churiwala | Corporate Vice President, AMD** **S. Ramachandran | Vice-Chancellor, Anurag University** **PA Govindcharulu | Director, Manjeera Digital Systems** **Srinivas Rao Mahankali | CEO, T-Hub** **Krishna Kanth | Director, ams OSRAM (Moderator)**			**5th Floor**
11:00	11:40	0:40	**IEEE CASS Young Professionals : Tea / Coffee Break and Poster Session 3***			**Ground Floor**
11:40	13:20	1:40	**IEEE CASS Young Professional: Talk on CAS Education Initiatives** **Session Chair: Chakradhar Adupa | SR University** **Ahmad Salahuddin Bin Mohd Harithuddin | Universiti Putra Malaysia** **Preet Yadav | R & D SoC Technical Program Manager, NXP** **Alex James | Professor, Digital University Kerala** **PA Govindacharulu | Director, Manjeera Digital Systems** **Vibhu | IEEE YP, IIT Roorkee** **Narendra Dhakad | IEEE YP, IIT Indore**	**Technical Papers Session: 5B** **Sensory & Biomedical Circuits and Systems** **Session Chair: Shiv Govind Singh | IIT Hyderabad** **99:** Comparative Analysis of SPAD Equivalent Models for Low-Light Imaging [Harshith Nimmagadda (IIIT Hyderabad); Anshu Sarje (IIIT Hyderabad)]	**Technical Papers Session: 5C** **RF an Analog Techniques** **Session Chair: N. Venkatesh | Silicon Labs** **49:** A 197 dBc/Hz FoMT 24.8-28.97 GHz Class-F VCO using Single-Turn Multi-Tap Inductor [Anik Batabyal (IIT Bombay); Rajesh Zele (IIT Bombay)]	**Session 1 & 2: 5th Floor** **Session 3: 6th Floor**
				149: A High-impedance 3-MOSFET Pseudo-resistor for Biomedical Amplifiers [Feng Yan (Sun Yat-Sen University); Kangkang Sun (Sun Yat-Sen University); Zhipeng Li (Sun Yat-Sen University); Jian Guan (Sun Yat-Sen University); Bingjun xiong (Sun Yat-Sen University); Jingjing Liu (Sun Yat-Sen University)]	**134:** Analysis of Switched-RC N-path filters with Finite Switch Resistance and Switched Gm-C filters using the Adjoint Network [Endersh Soni (Indian Institute of Technology , Roorkee); Saravana Manivannan (Indian Institute of Technology Roorkee)]	
				100: Implementation and Comparative Analysis of flexible Micro-Heater Circuits for Lab-on-a-chip Applications [Vikranth Varma Kosuri (IIIT Hyderabad); Anjali Singh (IIIT Hyderabad); Anshu Sarje (IIIT Hyderabad)]	**166:** A Low-Loss, Compact Wideband True-Time-Delay Line for Sub-6GHz Applications using N-Path Filters [MOHMAD AASIF BHAT (IIT Kanpur); IMON MONDAL (IIT Kanpur)]	
				163: Deep Learning Based Portable Respiratory Sound Classification System [Adithya Sunil Edakkadan (International Institute of Information Technology, Hyderabad); Abhishek Srivastava (IIIT Hyderabad)]	**256:** Modified Gm-Free Assisted Opamp Technique in Continuous Time Delta Sigma Modulators [Sayan Banerjee (Indian Institute of Technology, Delhi); Ankesh Jain (Indian Institute of Technology, Delhi)]	
				165: Smartphone-based Portable Blood Parameter Sensing using Machine Learning [Sangeeta Palekar (Research Scholar); Jayu Kalambe (Associate Professor, Biomedical Engineering)]	**20:** A Self-Biased Subthreshold CMOS Voltage Reference With Temperature Compensation Circuit For IoT Self-powered Sensor Applications [Yuxuan Huang (Sun Yat-Sen University); Feng Yan (Sun Yat-Sen University); Kangkang Sun (Sun Yat-Sen University); Jingjing Liu (Sun Yat-Sen University)]	
13:20	14:20	1:00	**IEEE CASS Young Professionals : Networking, Design Contest Demonstration (Ground Floor) & Lunch Break (5th Floor)**			**5th Floor**
				Technical Papers Session: 6B **Sensory & Biomedical Circuits and Systems** **Session Chair: J.V.R Ravindra | Vardhaman College, India** **226:** Low Precision Floating Point Spectral Feature Extraction Engine for Closed-loop Neuromodulation [Poulami Mandal (IIT Bombay); Sagar Mahajan (IIT Bombay); Laxmeesha Somappa (IIT Bombay)]	**Technical Papers Session: 6C** **ADCs and References** **Session Chair: Shanthi Pavan | IIT Madras** **121:** A 2.6-GHz I/O Buffer for DDR4 & DDR5 SDRAMs in 16-nm FinFET CMOS Process [Jhih-Ying Ke (National Sun Yat-Sen University); Lean Karlo Santos Tolentino (National Sun Yat-Sen University); Cheng-Yao Lo (National Sun Yat-Sen University); Tzung-Je Lee (National Sun Yat-Sen University); Chua-Chin Wang (National Sun Yat-Sen University)]	
				229: Noise Efficient Three Channel Amplifier for MEMS Cantilever Readout [Sebastian Simmich (University of Kiel); Patrick Wiegand (University of Kiel); Robert Rieger (University of Kiel)]	**4:** A 3.38-ppm/°C Voltage Reference for Harsh Environment Applications Empowered by the In-Loop Resistance Trimming Technique [Haonan Fan (Southeast University); Zhongyuan Fang (Southeast University); Yongjia Li (Southeast University); Qinsong Qian (Southeast University); Xiaozhi Kang (Fusion Semi Ltd., Shanghai); Minggang Chen (Southeast University); Weifeng Sun (Southeast University)]	

14:20	16:00	1:40	**Startup Forum (PRIME Asia)** **Session Chair: Rajesh Kumar Adla | T-Hub** **Rijin John | CEO, Maker Village** **Srinivas Rao Mahankali | CEO, T-Hub** **Sunil Maddikatla | Founder & CEO, Blue Semi** **Venkata Simhadri | CEO, ASIP Tech** **R Sai Chandra Teja | COO, Green PMU Semi**	**244:** Sensor Node with Position Validation towards Camptocormia Measurement at Home [Kamran Naderi Beni (University of Kiel); Matthias Christoph Eger (University of Kiel); Nils G. Margraf (University Hospital Schleswig-Holstein); Robert Rieger (University of Kiel)]	**158:** High-Precision Open-Loop Time Amplifier Using Current Regulator [Yusuke Toyoshima (KagoshimaUniversity); Ryosuke Kamiya (Kagoshima University); Kenichi Ohhata (Kagoshima University)]	**Session 1 & 2: 5th Floor** **Session 3: 6th Floor**
				249: Implementation of FFT using Low-Precision Floating Point for Rapid High Precision MEMS Readouts [Hitesh Kumar Sahu (IIT Bombay); Emon Sarkar (IIT Bombay); Laxmeesha Somappa (IIT Bombay)]	**184:** A Cryogenic Voltage Regulator with Integrated Voltage Reference in 22 nm FDSOI Technology [Alfonso Cabrera-Galicia (Forschungszentrum Jülich / ZEA2); Arun Ashok (ForschungszentrumJülich/ZEA2); Patrick Vliex (ForschungszentrumJülich/ZEA2); Andre Kruth (ForschungszentrumJülich/ZEA2); André Zambanini (ForschungszentrumJülich/ZEA2); Stefan van Waasen (ForschungszentrumJülich/ZEA2)]	
				251: Efficient CORDIC Architectures for FFT Based All Digital Resonator Frequency Estimation [Pushkar Sathe (Indian Institute of Technology Bombay); Ajay Verma (Indian Institute of Technology Bombay); Laxmeesha Somappa (IIT Bombay)]	**167:** A Robust Overdesign Prevention Circuit Technique Under Widely Varying Ambient Conditions [Mayank Anupam (Indian Institute of Technology, Kanpur); Imon Mondal (Indian Institute of Technology, Kanpur)] **197:** A novel architecture with nullified parasitic capacitance for accurate FuSa detection [Anup Deka (Intel); Biswarup Rana (Intel); Shuvoshree Bhattacharya (Intel)]	
16:00	16:30	0:30	**Tea / Coffee Break and Poster Session 4***			**Ground Floor**
16:30	17:50	1:20	**Technical Papers Session: 7A** **Analog and Power Management** **Session Chair: Ashudeb Dutta | IIT Hyderabad**	**Technical Papers Session: 7B** **Sensory & Biomedical Circuits and Systems** **Session Chair: JVR Ravindra | Vardhaman College**	**Technical Papers Session: 7C** **Signal Processing and CAD** **Session Chair: PA Govindacharulu | Manjeera Digital Systems**	**Session 1 & 2: 5th Floor** **Session 3: 6th Floor**
			78: A Novel Low-Power Shift-Register Controller for Digital Low-Dropout Regulators [Kartikay Tripathi (Indian Institute of Technology Roorkee); Madhav Pathak (IOWA State University); Sanjeev Manhas (IIT Roorkee); Anand Bulusu (IIT Roorkee)]	**265:** Efficient Dilution of a Fluid from its Related Arbitrary Stock Solutions using MEDA Biochips [Surya Naga Aditya V. Dupukuntla (IIT Roorkee, India); Koushik Sai Nimmaturi (IIT Roorkee, India); Tamal Mandal (IIT Roorkee, India); Sathwik Abramoni (IIT Roorkee, India); Sudip Roy (IIT Roorkee)]	**202:** Sub-nanosecond Delay High Voltage Level Shifter in 0.18µm HV-CMOS Technology for Cryo-Cooler Electronics [Nishant Kumar (SpaceApplicationsCentre); Hari Shanker Gupta (Space Applications Centre); Nihar Mohapatra (Associate Professor); Nilesh M. Desai (Space Applications Centre)]	
			148: A 95-nA quiescent-current fast-transient output-capacitor-less LDO with enhanced load regulation for IoT applications. [Raghav Bansal (Indian Institute of Technology Delhi); Shouri Chatterjee (Indian Institute of Technology Delhi)]	**266:** An 8-Channel TDM Spectral Feature Extraction for Neuromodulation SoC [K Akhilesh Rao (Indian Institute of Technology Bombay); Laxmeesha Somappa (IIT Bombay)]	**214:** Exploiting Node Level Algorithm Diversity for Distributed Compressed Sensing [Ketan Bapat (IIT Kharagpur); Mrityunjoy Chakraborty (IIT Kharagpur)]	
				191: Large Network of Wide-Range Analog Voltage Observers for Debug & Testability [Tapas Nandy (Intel Corporation); Ashish Joshi (Intel Corporation); Sanjoy Kumar Dey (Intel Corporation)]	**105:** V2Va: An Efficient Verilog-to-Verilog-A Translator for Accelerated Mixed-Signal Simulation [Yicong Shao (Shanghai Jiao Tong University); Chao Wang (Shanghai Jiao Tong University); Wangzilu Lu (Shanghai Jiao Tong University); Zhiwen Gu (Shanghai Jiao Tong University); Longfan Li (Shanghai Jiao Tong University); Jiajie Huang (Shanghai Jiao Tong University); Yuhang Zhang (Shanghai Jiao Tong University); Wei Mao (Hangzhou Institute of Technology, Xidian University, Hangzhou, China); Yongfu Li (Shanghai Jiao Tong University)]	
					39: A Transient-Enhanced Capacitor-Less LDO With 30-MHz Bandwidth and High Slew Rate [Wangchen Fan (Southeast University, Nanjing, China); Zhongyuan Fang (Southeast University); Yongjia Li (Southeast University, Nanjing, China); Minggang Chen (Southeast University); Weifeng Sun (Southeast University, Nanjing, China)]	
17:50	18:20	0:30	**Networking Break & Conference Closing Ceremony**			**5th Floor**

Poster Session 1
61: Modelling the Effect of Output-Dependent Integrator Gain on the Unadjusted Error of Inverter based 1st Order ΣΔ ADC Ashish Joshi, Tapas Nandy, Aashish T R, Mayank Devam and Sanjoy Kumar Dey
70: A 0.6V 10-bit 20kHz Capacitor Splitting Bypass Window SAR ADC for Biomedical Applications Kangkang Sun, Feng Yan, Huan Wu and Jingjing Liu
254: Design of a Wideband 8-20 GHz Receiver Front-End with Reduced Local Oscillator Phase-Error in 4-Path Mixer Arpit Sahni and Abhishek Srivastava
257: Mismatch Tolerant Negative Conductance Load Tuning for High Gain OTAs Mayur Marinaik and Naveen Kadayinti
273: A Current-mode Bandgap Reference with wideband PSRR better than 70dB from -40ºC to 75ºC Tarun Varma Sagiraju and Krishna Kanth Avalur
174: Surrogate-Assisted Metaheuristic Approach for Fast Variability Analysis Joel Thomas and Jai Narayan Tripathi
113: 2-Level Miller Detection-based High Side Gate Driver Design for Power MOSFETs Oliver Lexter July A. Jose, Jui-Min Kuo, Venkata Naveen Kolakaluri, Ming-Chin Mitch Chou and Chua-Chin Wang
Poster Session 2
19: Multiplexer & Memory Efficient Bit-Reversal Algorithms Basamgari Bhanu Prakash Reddy, Nitish Kumar, Kavindra Kandpal and Manish Goswami
46: A1RL: Approximate 1-row-LUT-based Low-power signed Multipliers for DSP and Machine learning applications on FPGAs Zainab Aizaz, Kavita Khare and Aizaz Tirmizi
55: Double Gate JLT Based New TIGFET for Dynamic C2MOS Application Tika Pokhrel and Alak Majumder
203: A MATE-GDBF Algorithm for Irregular Punctured LDPC Codes and Its Decoder Implementation Xiao-Juan Huang, Li-Wei Liu, Yen-Chin Liao, Hsie-Chia Chang and Sau-Gee Chen
224: Analyzing Area and Latency Overhead in C and RTL Locked Designs Divyanshu Nauni, Chandan Karfa and Praveen Karmakar
264: On a Piecewise Linear Function Approximation for Quantum Computation Hideaki Okazaki
223: Real-Time Zero-Phase Digital Filter Using Recurrent Nueral Network Tantep Sinjanakhom and Sorawat Chivapreecha
Poster Session 3
10: Architectural Exploration of Heterogeneous FPGAs for Performance Enhancement of ML Benchmarks Anubhav Mishra, Nanditha Rao, Ganesh Gore and Xifan Tang
94: Programmable Binary Weighted Time-Domain Vector Matrix Multiplier for In-Memory Computing Bipul Boro, Ashvinikumar Dongre, Rushik Parmar and Gaurav Trivedi
176: On edge FPN reduction in CMOS Image Sensor using CNN with Attention Mechanism Sandeep Kodam, Wilfred Kisku, Amandeep Kaur and Deepak Mishra
186: High Throughput Hardware Acceleration for Image Generation using HLS BhanuPrasad A and Kuruvilla Varghese
187: An Intelligent CMOS Image Sensor System Using Edge Information for Image Classification Wilfred Kisku, Prateek Khandelwal, Amandeep Kaur and Deepak Mishra
208: NDIE: A Near DRAM Inference Engine Exploiting DIMM's Parallelism Palash Das and Hemangee Kapoor
Poster Session 4
LB_3: An Energy Efficient C-2C Charge-Sharing Based Analog Compute-In-Memory Architecture Dinesh Kushwaha, Rajat Kohli, Jwalant Mishra, Jainendra Singh, Rajiv Joshi, Sudeb Dasgupta and Anand Bulusu
LB_18: Exploring Early Timing Insights: The Impact of Parasitic Methodology Subba Ramkumar Reddy Annapalli, Lakshmi Sarvaani Pallapu, Kritika Das and Vikramkumar Pudi
LB_28: A Sensing Device For Highly Efficient Real-Time Road Condition Monitoring and Drive Assisstance System Qadeer Khan and Aarya Sumuk
44: Biochemical Blood sensing with Colorimetric Image Analysis with Biodegradable Flow Cell Sangeeta Palekar, Jayu Kalambe and Rajendra M. Patrikar
196: ECG artifacts suppression using the NLSRA-based cascaded fixed point interference canceller MohammedMujahid UllaFaiz, Azzedine Zerguine and Izzet Kale
204: Energy Harvester Powered Fully Digital ECG Front End Acquisition with Integrated TDC Purvi Patel and Biswajit Mishra